In the claims:

Claims 1 to 14 (canceled)

15. (currently amended) A semiconductor device structure comprising:

a first metallic interconnect;

a second metallic interconnect~~;~~ having a primary via structure, said primary structure having an active diffusion volume relative to a location within the primary structure wherein voids can be located~~,~~ disposed between and electrically intercoupling the first and second metallic interconnects; and

a buffer structure~~,~~ disposed upon the ~~first~~ second metallic interconnect in proximity to the primary via structure~~, and adapted~~ and within the diffusion volume to buffer the primary via structure from diffusive voiding occurring at a contact point between the primary via structure and the ~~first~~ second metallic interconnect.

16. (currently amended) The structure of claim 15 wherein the first ~~second~~ metallic interconnect and the primary via structure are copper- based dual damascene structures.

17. (previously presented) The structure of claim 15 wherein the buffer structure comprises a second via structure, disposed between and electrically intercoupling the first and second interconnects.

18. (currently amended) The structure of claim 15 wherein the buffer structure comprises a second, electrically inactive, via structure, disposed upon the second ~~first~~ metallic interconnect proximal to the primary via structure and within the active diffusion volume.

19. (currently amended) The structure of claim 18 wherein the buffer structure comprises an electrically inactive structure disposed upon the second ~~first~~ metallic interconnect to immediately and completely surround~~ing~~ the primary via structure.

20. (previously presented) The structure of claim 15 wherein the buffer structure comprises:

a second via structure, disposed between and electrically intercoupling the first and second metallic interconnects; and

a third electrically inactive, via structure, disposed upon the second ~~first~~ metallic interconnect proximal to the primary via structure.

21. (new) A semiconductor device for decreasing diffusive damage effects to a location within a primary structure, comprising:

a primary structure having an active diffusion volume relative to a location within the primary structure wherein voids can be located; and

a redundant structure within the active diffusion volume to minimize movement of voids to said location.

22. (new) The device of claim 21 wherein the redundant structure comprises plural redundant structures.

23. (new) The device of claim 21 wherein the redundant structure is operative relative to diffusive redundancy only.

24. (new) The device of claim 21 wherein the redundant structure is operative relative to electrical redundancy.

25. (new) The device of claim 21 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate

26. (new) The device of claim 22 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate

27. (new) The device of claim 23 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate

28. (new) The device of claim 24 wherein said device has a copper-based, dual-damascene structure having an active diffusion volume within the dual-damascene structure relative to a location within the dual-damascene structure to which voids can migrate

29. new) 29.. A semiconductor device to minimizing diffusive damage effects comprising:

a first layer of interconnect material and a second layer of interconnect material partially overlapping said first layer of interconnect material and coupled to said first layer of interconnect material by a via;

an active diffusion volume in said first layer of interconnect material within which voids can be located; and

a structure in said first layer within said active diffusion volume to minimize migration of said voids toward said via.

30.. (new) The device of claim 29 wherein said structure is at least one via extending from said first layer and spaced from said second layer.

31. (new) The device of claim 30 wherein said at least one via is a plurality of vias.

32. ()new) The device of claim 31 wherein said plurality of vias are equidistant from said via and spaced apart.

33. (new). The device of claim 29 wherein said structure is at least one electrically insulating slot disposed in said first layer and within said active diffusion volume.

34. (new) The device of claim 24 wherein said at least one slot is a plurality of spaced apart slots.

35. (new) The device of claim 29 wherein said structure further includes at least one electrically insulating slot disposed in said first layer and within said active diffusion volume.